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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,614	LIN, FENG	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-75* is/are pending in the application.

4a) Of the above claim(s) *31-33 and 35-75* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-30 and 34* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's response to the restriction requirement filed on 11/14/02 has been received and entered in the case. The election of Group I for prosecution without traverse is acknowledged. The following is a detailed Office Action of the elected claims, i.e., claims 1-30 and 34.

Drawings

2. The drawings are objected to because in Fig. 6, the decision block 80d has only one output, i.e., it should have two outputs, Yes and No. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because:

(i) it uses words which can be implied, i.e., "is disclosed" on line 3,

(ii) it has more than 150 words.

Correction is required. See MPEP § 608.01(b).

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the terms "measuring delay line input", "measurement delay line", "measurement delay line output", "variable delay line input", ..., used in claim 19 are not seen in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19-22 and 26-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 19, the recitation on lines 2-4 is misdescriptive, i.e., it does not make any sense to recite an input node connected to a signal and an output node connected to different signals, a node should receive a signal, not connect to a signal, and if a node receives two different signals, a selection circuit must be recited. The limitation recited on lines 5-8 is unclear

due to the antecedent basis problem discussed in section 5 herein above. The limitation recited on lines 12-16 is unclear due to the antecedent basis problem discussed in section 5 above. The Applicant is requested to match each term used in the claim with the element(s) shown in the drawings. The term "the signals" on line 12 lacks clear antecedent basis, i.e., it is unclear which signals they are referring to. The term "the circuit" recited on line 14 lacks antecedent basis. The claim is further rejected because it is an incomplete claim since the claim does not have a logical structural relationship between recited elements, a merely listed elements without any recitation to particularly point out a relationship between elements fails to satisfy the 112, second paragraph requirement.

As per claims 20-22, these claims are indefinite because of the indefiniteness of claim 19.

As per claim 26, the recitation that the phase detector receives the inverted clock input signal is misdescriptive because as shown in Fig. 1, the CIN' signal is not received by the phase detector. The claim is further rejected for being an incomplete claim because the recited function selectively feeds CIN and CIN' into the SMD is not supported by the recited elements, i.e., none of the recited elements supports the recited function.

As per claims 27-30, these claims are indefinite because of the indefiniteness of claim 19.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in

section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-11, 13-30 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,166,990, issued to Ooishi et al.

As per claim 13, Ooishi discloses a memory device (Fig. 39), comprising:

a synchronous mirror delay (SMD) circuit (the circuit 83, details is in Fig. 41), and

a phase detector (the circuit 85, details of the phase detector is in Fig. 43, the phase comparison circuit 100) connected to the SMD (Fig. 39, the circuit 85 is connected to the circuit 83), the phase detector receiving a clock input signal RFCK (node D) and a clock delay signal (node E), the clock input signal and the clock delay signal each having timing characteristics (the timing characteristics are shown in Fig. 44, node D and node E waveforms), the phase detector outputting a pair of branches (Fig. 43, UP and DWN) each having a logical level (Fig. 44, high or low), wherein the logical levels of the branches define a plurality of conditions of the clock input signal and the clock delay signal based on the timing characteristics (depending on the logical levels of the UP and DWN signals), and wherein at least one of the conditions reduces a number of effective delay stages in the SMD (column 38, lines 32-35).

As per claim 14, the recited limitation is merely the definition of the clock input signal CIN, and since the Ooishi's clock input signal RFCK can be defined as recited, the recited limitation is met.

As per claims 15-17, the recited limitations are merely the results when the Ooishi's circuit operates, and therefore, the recited results will be met when the Ooishi's circuit operates, i.e., the TUP and TDWN signals controls the number of effective delay stages in the SMD.

As per claim 18, Ooishi discloses a synchronous mirror delay system (Fig. 39), comprising:

a synchronous mirror delay (SMD) circuit (the circuit 83, details is in Fig. 41), and

a phase detector (the circuit 85, details of the phase detector is in Fig. 43, the phase comparison circuit 100) connected to the SMD (Fig. 39, the circuit 85 is connected to the circuit 83), the phase detector receiving a clock input signal RFCK (node D) and a clock delay signal (node E), the clock input signal and the clock delay signal each having timing characteristics (the timing characteristics are shown in Fig. 44, node D and node E waveforms), the phase detector outputting a pair of branches (Fig. 43, UP and DWN) each having a logical level (Fig. 44, high or low), wherein the logical levels of the branches define a plurality of conditions of the clock input signal and the clock delay signal based on the timing characteristics (depending on the logical levels of the UP and DWN signals), and wherein at least one of the conditions reduces a number of effective delay states in the SMD (column 38, lines 32-35);

the limitation recited on lines 9-15 is met for the same reason noted in claim 14;

the limitations recited on lines 16-17 are met since it is merely the result when the circuit operates, i.e., by reducing the number of effective delay stages in the second phase and by bypassing the SMD in the third and fourth phases, the optimum phase latching in the shortest time is achieved by the Ooishi's circuit.

As per claim 19, Ooishi discloses a synchronous mirror delay circuit (Fig. 39) for use with an external clock signal (the external clock signal which provides the ECLK clock and the not(ECLK) clock at nodes 75a and 75b), comprising (due to the indefiniteness problem discussed

herein above, the following rejections based on the best guess by the examiner, changes to overcome the rejection may constitute new ground of rejections necessitated by the changes):

an input buffer (not shown) having an input connected to the external clock signal and an output connected to a clock input signal ECLK, an inverted clock input signal not(ECLK) and a clock delay (at node E) each having timing characteristics;

a synchronous mirror delay (the circuit 83) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line. the variable delay line including a variable delay line output (the circuit 83 receives the inputs TUP, TDWN and outputs the clock signal CLK0); and

a phase detector (the circuit 85) disposed between the input buffer and the synchronous mirror delay, the phase detector having a first input for receiving the CIN (node D), a second input for receiving the CDLY (node E), the phase detector generating one of a plurality of output signal combination (Fig. 43, UP, DWN) , each combination responding to a phase of the signals based on the timing characteristics, a CDLY SMD input connected to the measurement delay line input (Fig. 41, the SMD circuit receives inputs and output the signal CLK0), and an SMD output connected to the variable delay line output (as shown in Fig. 41), the circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals (either the ECLK or the not(ECLK) is selected), and wherein at least one of the phases reduces a number of effective delay stages of the SMD (this is the reason why the Ooishi circuit is invented).

As per claims 20-22, these claims are rejected for the same reasons noted in claims 15-18.

As per claim 23, this claim is rejected for the same reasons noted in claim 18 discussed herein above.

As per claim 24, the recited condition is met when the Ooishi's synchronous mirror delay system operates.

As per claim 25, this claim is rejected for the same reason noted in claim 18.

As per claim 26, this claim is rejected for the same reasons noted in claim 13, and further, the recited logic reads on the circuits 102 and 106 shown in Fig. 43, and the recited limitations on the last three lines are met since they merely recite the operation of the circuit. The recited CIN reads on the ECLK clock and the recited CIN' reads on the not(ECLK) clock.

As per claim 27-30, these claims are rejected for the same reasons noted in claims 14-17, respectively.

As per claim 34, this claim is rejected for the same reasons noted in claim 13 above, and further, the limitations recited on lines 2-7 are merely standard features in a computer system, and since the Ooishi circuit shown in Fig. 1 is for a memory circuit in a computer system, the recited limitations are met, the recited logic reads on the circuits 102 and 106 shown in Fig. 43, and the recited limitations on the last four lines are met since they merely recite the definition of the clock input signal CIN and the operation of the circuit.

As per claim 1, this claim is merely a method to operate a SMD circuit having elements and connections shown in Fig. 39, since Ooishi teaches the circuit as discussed in detailed in claim 18 above, he inherently teaches the recited steps. A comprehensive steps are further disclosed when reading the operation of the circuit shown in Fig. 39.

As per claims 2-4, these claims are discussed in claims 14, 16 and 17, respectively.

As per claims 5-11, these claims are rejected for the same reasons noted in claims 34, 34, 18, 14, 34, 34, 14, respectively.

Allowable Subject Matter

8. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 is allowable because the prior art of record fails to disclose or suggest a method of reducing effective delay stages in a SMD circuit which includes a step of selecting as an output clock signal the CIN signal or the signal from the SMD output using a multiplexor.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Nos. 6,373,913, 6,018,259, and 5,771,264 disclose various circuits and methods to control the timing of the SMD circuits which can be used to reject some of the recited claims.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
December 27, 2002